UM0858
User manual

Getting started with STEVAL-PCC011V1, ST802RT1 FX mode Ethernet PHY demonstration kit

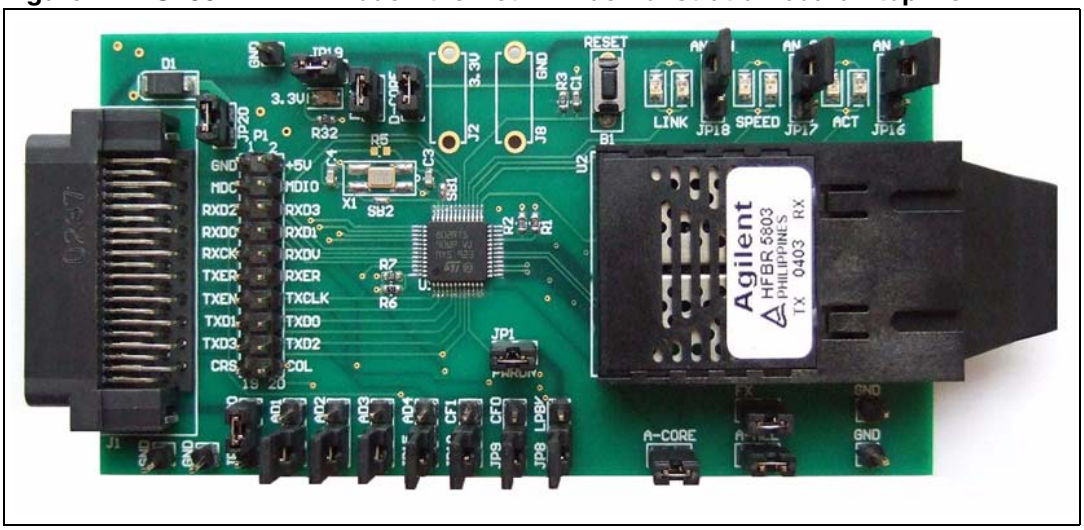
1 Introduction

The STEVAL-PCC011V1 demonstration kit was designed to evaluate the ST802RT1 FX mode. This device is a Fast Ethernet physical layer (PHY) interface which supports 100 Base-FX applications. The PHY provides a Media Independent Interface (MII) and Reduced Media Independent Interface (RMII) for easy attachment to a 10/100 Media Access Controllers (MAC). The demonstration board features jumpers, test points and connectors to test the features provided by the ST802RT1 FX mode Ethernet PHY.

To quickly evaluate the microcontroller and physical layer, the device can be connected to the STM32F107 controller demonstration board through an additional header connector. The controller board is preprogrammed with a web server demonstration. The STM32F107 controller demonstration board is not part of the STEVAL-PCC011V1 package but has to be purchased separately. The only way to get it is to purchase additionally STEVAL-PCC010V1.

The board can be equipped with a dedicated digital connector compatible to the Spirent® Communications SmartBits 200/2000 (SMB-200/ SMB-2000) analysis system.

Figure 1. ST802RT1 FX mode Ethernet PHY demonstration board - top view



This document refers to STEVAL-PCC010V1 user manual UM0819 which provides a complete description of the ST802RT1 Fast Ethernet physical layer interface in TX mode. For a complete description of the ST802RT1 transceiver, please refer to the datasheet.

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2 Board key features

ST802RT1 FX mode Ethernet PHY demonstration board has the following features:

- ST802RT1 FX mode Fast Ethernet physical layer transceiver
- On-board 3.3 V LDO regulator
- On-board 25 MHz crystal
- 12 jumpers for bootstrap configuration (MII address, auto-negotiation, loopback, power-down, MII/RMII configuration)
- Several GND test points and jumpers for power consumption measurement
- Connectors
  - 20-pin full pitch header connector for debug purposes (compatible to the STM32F107 controller board)
  - 40-pin connector compatible to the Spirent Communications SmartBits 200/2000 (SMB-200/ SMB-2000) analysis system (not assembled)
  - Optical transceiver connector.

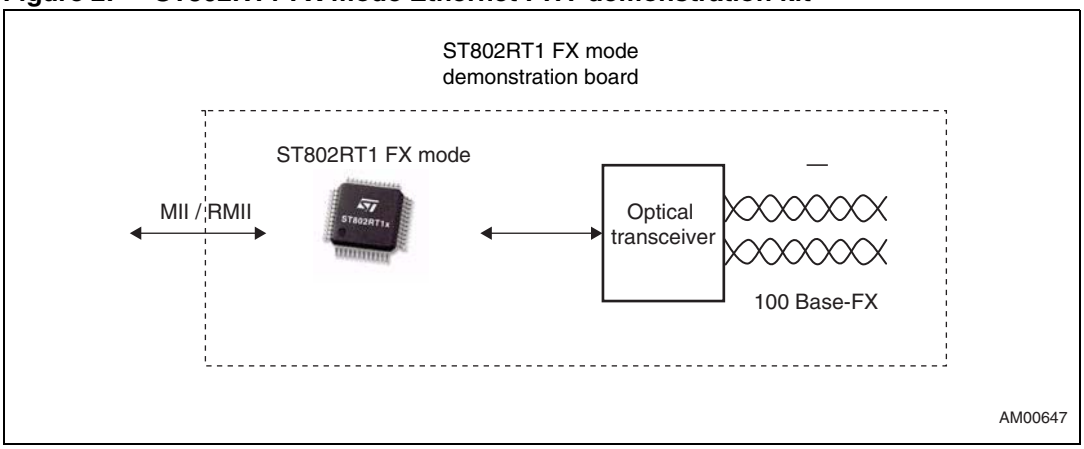
3 General system description

The ST802RT1 FX mode STEVAL-PCC011V1 demonstration board was designed to evaluate the PHY chip in fiber optics mode. It therefore allows to easily select the PHY boot options, to evaluate the power consumption of the chip and to attach the device to the professional test equipment.

The board also allows simple connection to the customer microcontroller or FPGA platforms by means of the on-board connectors. The board was designed to allow evaluation of MII and RMII digital communication interfaces.

In addition, the STM32F107 controller demonstration board can extend the ST802RT1 FX mode demonstration board with STM32™ microcontroller and its embedded MAC. This allows to evaluate application based on the embedded microcontroller and the Ethernet PHY in FX mode.

Figure 2. ST802RT1 FX mode Ethernet PHY demonstration kit



4 Package content

The ST802RT1 FX mode Ethernet PHY ST802RT1 demonstration kit includes the following items:

Hardware content

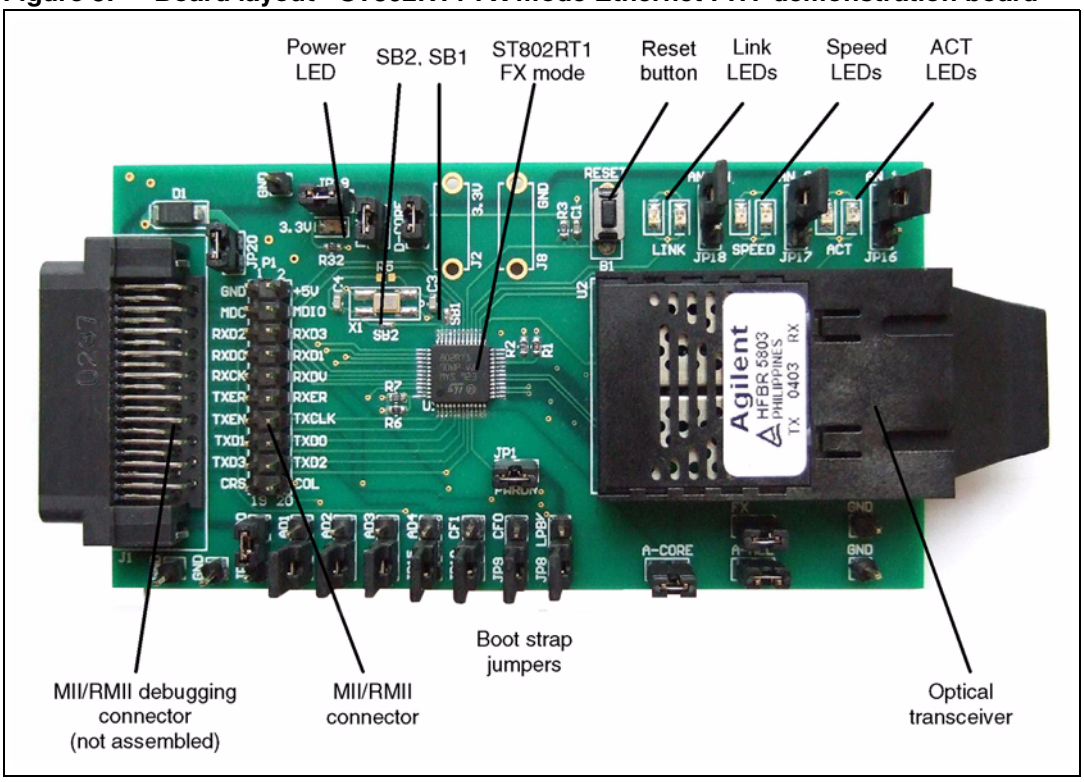
- One ST802RT1 FX mode Ethernet PHY demonstration board

Documentation

- ST802RT1 product documentation
- This user manual.

5 Board layout - ST802RT1 FX mode Ethernet PHY demonstration board

Figure 3. Board layout - ST802RT1 FX mode Ethernet PHY demonstration board



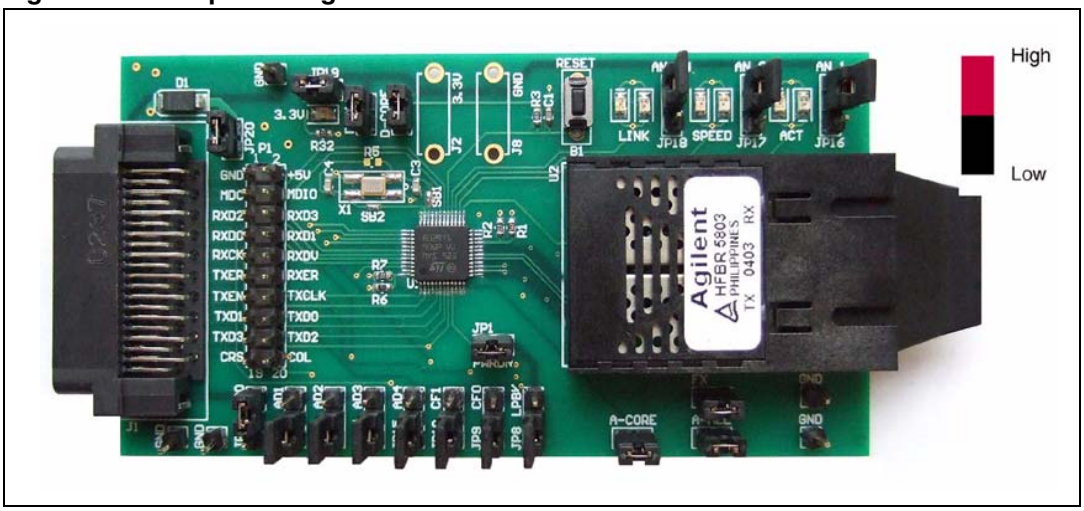
6 Configuration and functionality

This section describes the functions and configuration of the STM802RT1 FX mode Ethernet PHY demonstration board.

6.1 Configuration and functionality of ST802RT1 FX mode Ethernet PHY demonstration board

In this chapter jumper “high” means that the jumper is placed in the position closer to the top edge of the board and position “low” means that the jumper is placed in the position closer to the bottom edge of the board as shown by *Figure 4*.

Figure 4. Jumper configuration



6.1.1 Bootstrap options

The ST802RT1 FX mode PHY uses many of the functional pins as strap options. The values of these pins are sampled during hardware reset and power-up. They are used to strap signals on the device into specific modes of operation. The ST802RT1 FX mode provides a simple strap options to automatically configure the device to operate in the modes requiring no device register configuration. All strap pins have a weak internal pull-ups or pull-downs. To change the default strap value, the strap pins should be connected directly to V_{CC} or GND with an external 2.2 kΩ resistor. The software reset and power-down through the power-down pin cannot be used to change the strap configuration.

Auto-negotiation

Auto-negotiation functions are not supported in 100 Base-FX mode. It is possible to change the HW configuration of the involved pins - see *Table 1* for the default settings and check the board schematic for further possible connections.

Table 1. Auto-negotiation jumper settings for evaluation purpose only(1)

Jumper	Description	Default configuration
JP16	AN_1	High
JP17	AN_0	High
JP18	AN_EN	High

1. See functionality of AN_xxx pins in the ST802RT1 documentation.

PHY MII address

The MDIO/MDC serial management interface is used to access the internal registers of the PHY. The Ethernet MAC must know the PHY address to establish successful communications with it. Special case is PHY address 0x00. If this address is used as the bootstrap address during the reset, the 00000 value is latched into the internal receive mode control register RN14 (0x14h) and the PHY goes also to the isolation mode. It is possible to change the PHY address by writing the RN14 register when the application is already running.

Table 2. PHY MII address jumper settings

Jumper	Description	Default configuration
JP11	MII address 0	High
JP12	MII address 1	Low
JP13	MII address 2	Low
JP14	MII address 3	Low
JP15	MII address 4	Low

Power-down

This pin is an active low input of the PHY and should be asserted low to put the device in power-down mode. During the power-down mode, TXP/TXN outputs and all LED outputs are 3-state, and the MII interface is isolated. The power-down functionality is also achievable by software by asserting bit 11 of register RN00.

Table 3. Power-down jumper setting

Jumper	Description	Default configuration
JP1	Power-down, if fitted - PHY works normally; if not fitted - PHY is in power-down mode	Fitted

Loopback

Local loopback passes data internally from the transmitting to the receiving serial analog logic. There are two ways to enter the internal loopback mode, either writing RN00 register, bit 14 (MDIO/MDC) or by using bootstrap LPBK pin (V_{DD} - enabled, GND - disabled, through 2.2 kΩ resistor).

Table 4. Loopback jumper setting

Jumper	Description	Default configuration
JP8	LPBK - loopback; “high” - internal loopback selected (mainly for debug purposes); “low” - normal operation	Low

MII/RMII mode selection

A strapping option allows setting the operating mode of the MAC data interface. Default operation (no pull-ups) enables normal MII operating mode. Strapping CF0 “high” will cause the device to be in RMII.

Table 5. MII/RMII jumper settings

Jumper	Description	Default configuration
JP9	CF0 - MAC data interface selection	Low
JP10	CF1 - MAC data interface selection	Low

Table 6. MII/RMII interface selection

	CF0 (JP9)	CF1 (JP10)
MII	Low	X
RMII	High	Low

6.1.2 Solder bridges

The SB1 and SB2 solder bridges are used to connect 25 MHz crystal X1 to the ST802RT1 FX mode PHY. They can be removed to disconnect the crystal when external clock signal on test point MCO is used as the input clock.

6.1.3 RESET button

The RESET button resets the ST802RT1 FX mode PHY to its initial state.

6.1.4 LEDs

By default the LEDs have the following functionality:

Table 7. LEDs functionality - alternative 1

LED	Description	Details
LED1	BLINK for activity	JP16 is low
LED2	BLINK for activity	JP16 is high
LED3	ON for 100 Mb	JP17 is low
LED4	ON for 100 Mb	JP17 is high
LED5	ON for link up / OFF for link down	JP18 is low
LED6	ON for link up / OFF for link down	JP18 is high

Alternatively it is possible to change the meaning of LED1 - LED6 by writing the PHY register RN1B [0d27, 0x1B]:

Table 8. LEDs functionality - alternative 2

LED	Description	Details
LED1	ON for full duplex, BLINK for collision	JP16 is low
LED2	ON for full duplex, BLINK for collision	JP16 is high
LED3	ON for 100 Mb	JP17 is low
LED4	ON for 100 Mb	JP17 is high
LED5	ON for link up and BLINK for activity / OFF for link down	JP18 is low
LED6	ON for link up and BLINK for activity / OFF for link down	JP18 is high
LED8	Is used for indicating that the board is powered	—

6.1.5 Test point MCO

The test point MCO can be used to connect external clock signal to the clock input of the STM802RT1A PHY in MII mode. Note that the 25 MHz crystal X1 has to be disconnected from the ST802RT1 FX mode PHY by removing solder bridges SB1 and SB2 before connecting any external signal to the test point.

6.1.6 Power supply and power consumption measurement

The board was designed to be powered from the +5 V DC supply voltage coming from the P1 header connector or by means of JP20. On-board jumpers allow to measure the actual current power consumption of the Ethernet PHY chip and the power consumption of the peripheral components connected to the PHY. The typical total power dissipation of the board is 500 mW.

Table 9. Power supply jumpers

Jumper	Description	Details
JP3	Disconnects/connects the supply voltage from/to the optical transceiver (allows to measure power consumption of the optical transceiver)	Fitted
JP4	Disconnects/connects the digital domain supply voltage from the peripheral components around the PHY from/to the power supply	Fitted
JP5	Disconnects/connects the digital domain supply voltage of the PHY from/to the power supply	Fitted
JP6	Disconnects/connects the analog domain supply voltage from the peripheral components around the PHY from/to the power supply	Fitted
JP7	Disconnects/connects the analog domain supply voltage of the PHY from/to the power supply	Fitted
JP19	Connects the output of the on-board voltage regulator (U2) to the rest of the application board	Fitted
JP20	Connects the external power supply input (from pin 2 of connector P1) to the input of the on-board voltage regulator (U3)	Fitted

7 FX mode functionality

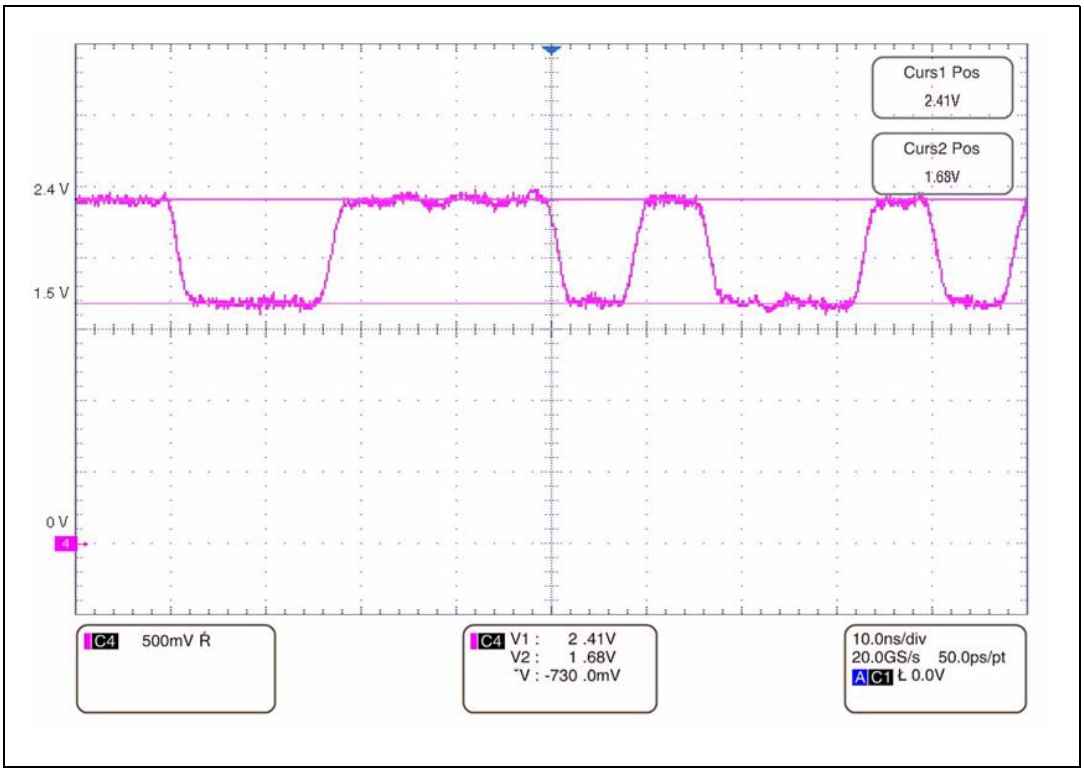
In this section you can find a short description of the functionality of the ST802RT1 Ethernet PHY in 100 Base-FX mode. ST802RT1 provides a low voltage pseudo ECL interface suitable for driving a fiber optic transceiver - communication between the PHY and the transceiver. The AFBR5803 optical transceiver allows to connect to the multimode fiber backbones.

7.1 LVPECL - low voltage pseudo emitter coupled logic

The ST802RT1 provides a low voltage pseudo ECL (LVPECL) interface suitable for driving a fiber optic transceiver. LVPECL is a differential signaling system mainly used in high speed systems. It requires a positive 3.3 V supply voltage. The LVPECL logical low level (LVPECLLOW) is approximately V_{CC}–1.7 V, the LVPECL logical middle level (LVPECLMID) is approximately V_{CC}–1.3 V and the LVPECL logical high level (LVPECLHIGH) is approximately V_{CC}–0.9 V.

Figure 5 shows a typical waveform of the low voltage PECL signal measured on the TXP pin of ST802RT1 in FX mode. The TXN signal would be inverted exactly with the reference to LVPECLMID voltage level.

Figure 5. ST802RT1- single ended measurement on the TXP line in 100 Base-FX mode



7.2 Utilization of ST802RT1 FX mode Ethernet PHY with AFBR-5803 optical transceiver

The following ST802RT1 PHY pins must be connected with the optical transceiver with respect to the LVPECL voltage levels.

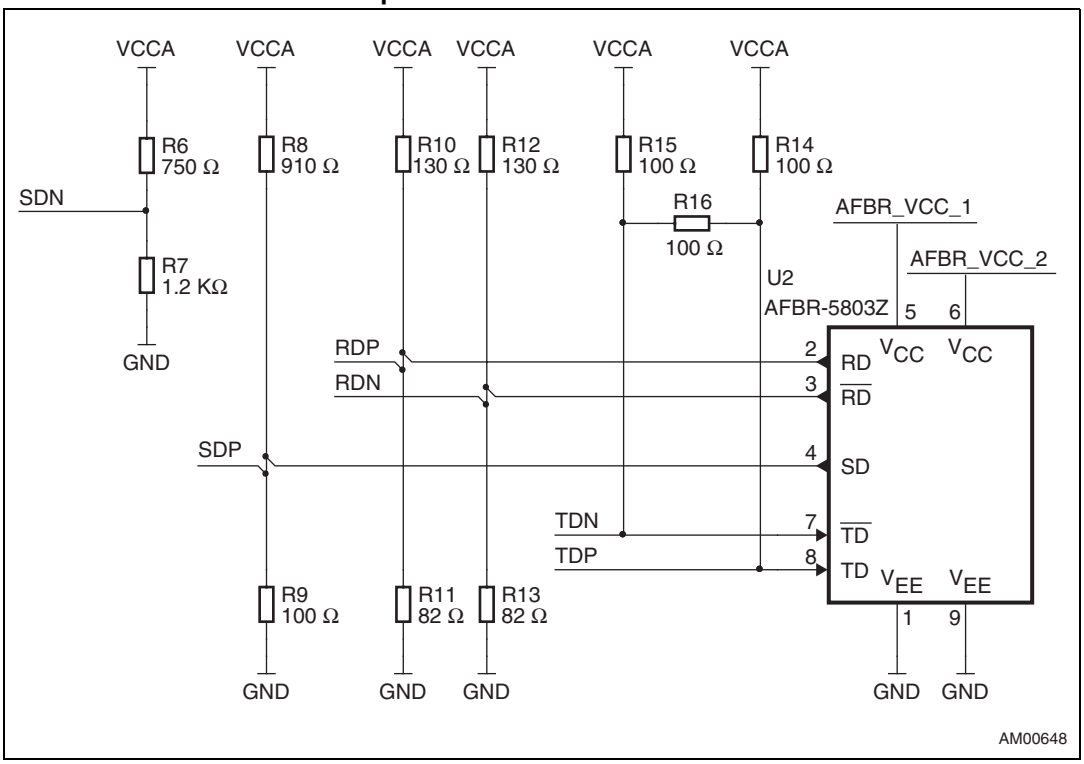
- SDP - positive signal detect - indicates the optical link status and is usually bonded out from the optical receiver.
- SDN - negative signal detect - pin SDN can be permanently connected to LVPECLMID because it is not usually bonded out from the optical transceiver
- TXP, TXN - differential transmit outputs
- RXP, TXN - differential receive inputs

Figure 6 shows the recommended connections of the Ethernet PHY ST802RT1 and the optical transceiver AFBR-5803. The SDN pin is connected to the voltage divider represented by resistors R6 and R7 and is not directly connected to the optical transceiver. Its voltage level is equal to LVPECLMID, that is 2.03 V.

Place a 100 Ω termination resistor directly across the TDP to TDN inputs of the optical transmitter. Connect a 100 Ω resistor between TXN and VCCA and between TXP and VCCA to achieve the pseudo emitter coupled logic (PECL) levels for the optical transmitter.

The RDN, RDP and SDP lines are connected to a resistor net with respect to the LVPECL logic, impedance characteristic of the optical transceiver and PHY and the recommended schematic for the used optical transceiver.

Figure 6. Recommended schematic for connection of ST802RT1 FX mode with AFBR-5803 optical transceiver



8 Connectors

8.1 Connectors of the ST802RT1 FX mode Ethernet PHY demonstration board

8.1.1 MII/RMII debugging connector J1

Figure 7. MII/RMII debugging connector J1

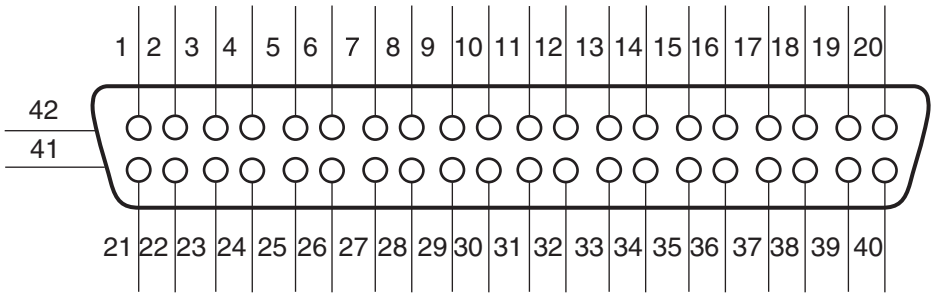


Table 10. MII/RMII debugging connector J1(1)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	+5 V	12	FXCLK	23	GND	34	GND
2	MDIO	13	FXEN	24	GND	35	GND
3	MDC	14	FXD_0	25	GND	36	GND
4	RXD_3	15	FXD_1	26	GND	37	GND
5	RXD_2	16	FXD_2	27	GND	38	GND
6	RXD_1	17	FXD_3	28	GND	39	GND
7	RXD_0	18	COL	29	GND	40	Not connected
8	RXDV	19	CRS	30	GND	41	GND
9	RXCLK	20	Not connected	31	GND	42	GND
10	RXER	21	+5 V	32	GND		
11	FXER	22	GND	33	GND		

1. This connector is not assembled by manufacturing.

8.1.2 MII/RMII connector P1

Figure 8. MII/RMII connector P1

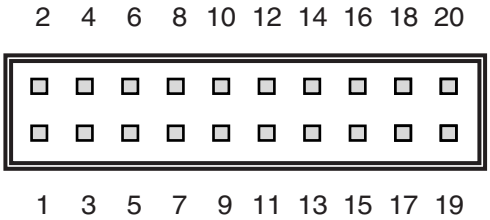


Table 11. MII/RMII connector P1

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	GND	6	RXD3	11	FXER	16	FXD0
2	+5 V	7	RXD0	12	RXER	17	FXD3
3	MDC	8	RXD1	13	FXEN	18	FXD2
4	MDIO	9	RXCLK	14	FXCLK	19	CRS
5	RXD2	10	RXDV	15	FXD1	20	COL

8.1.3 Optical transceiver U2

Figure 9. Optical transceiver connector U2

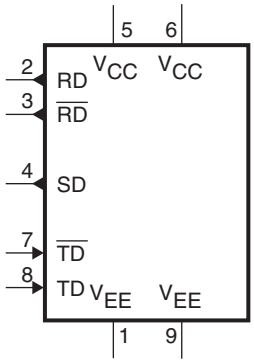


Table 12. Optical transceiver connector U2

Pin	Description	Pin	Description
1	GND	2	Receive data positive
3	Receive data negative	4	Signal detect
5	V_{CC} (+3.3 V)	6	V_{CC} (+3.3 V)
7	Transmit data negative	8	Transmit data positive
9	GND		

Appendix A ST802RT1 FX mode Ethernet PHY demonstration board - BOM and schematic

Table 13. Bill of material

Designator	Quantity	Description	Value	Order	Not assemble
B1	1	Push button (DT2112C)	RESET	GM Electronic®: 630-121 Farnell: 9471898	
C1, C2	2	Capacitor	10 nF	Farnell: 1709948	
C3, C4	2	Capacitor	12 pF	Farnell: 1462447	
C5, C6, C7, C9, C11, C14, C15, C18, C20	9	Capacitor	100 nF	Farnell: 4532004	
C8, C12	2	Capacitor	1 µF / X5R Murata GRM188R60J105KA01	Murata: GRM188R60J105KA01 Farnell: 1710296	
C13, C16, C19, C21	4	Polarized capacitor	10 µF / tantalum	Farnell: 1213794	
D1	1	Schottky diode	STPS160A / STPS2L40U	STMicroelectronics™: STPS2L40UF	
J1	1	Plug assembly, 40-pin connector	Connector 40	Tyco Electronics: 174218-2; Fujitsu: FCN-238P040-G/F	J1
J2, J8	2	1-pin header, 2 mm banana receptacle	2MM_REC		J2, J8
J3, J4, J5, J6, J7	5	1-pin header	GND	Farnell: 1593411	
JP3, JP6, JP7, JP1, JP4, JP5, JP19, JP20	8	2-pin jumper wire	Jumper	Farnell: 1593411	
JP8, JP9, JP10, JP11, JP12, JP13, JP14, JP15, JP16, JP17, JP18	11	3-pin jumper wire	Jumper3	Farnell: 1593412	
L1, L2, L3, L4	4	Ferrite bead	NFE31PT222Z1E9L Murata	Farnell: 9528172	
LED1, LED2	2	LED	Yellow	Farnell: 1226420	
LED3, LED4, LED8	3	LED	Red	Farnell: 1226392	
LED5, LED6	2	LED	Green	Farnell: 1226373	
P1	1	Header, 20-pin, dual row	Header 10 x 2	Farnell: 1593446	
R1	1	Resistor	5.6 KΩ	Farnell: 1514773	

Table 13. Bill of material (continued)

Designator	Quantity	Description	Value	Order	Not assemble
R2	1	Resistor	91 KΩ	Farnell: 1646361	
R3, R4	2	Resistor	10 KΩ	Farnell: 1601277	
R5	1	Resistor	1M NA	Farnell: 1631320	R5
R6	1	Resistor	750 Ω	Farnell: 1399909	
R7	1	Resistor	1.2 KΩ	Farnell: 1632396	
R8	1	Resistor	910 Ω		
R9, R14, R15, R16	4	Resistor	100 Ω		
R10, R12	2	Resistor	130 Ω		
R11, R13	2	Resistor	82 Ω		
R17, R18, R19, R20, R21, R22, R23, R24	8	Resistor	2.2 KΩ	Farnell: 1632417	
R25	1	Resistor	330 Ω	Farnell: 1646224	
R26, R28, R30	3	Resistor	2 KΩ	Farnell: 1632414	
R27, R32	2	Resistor	470 Ω	Farnell: 9367659	
R29	1	Resistor	220 Ω	Farnell: 1646159	
SB1, SB2, SB3	3	Soldering bridge	Soldbridge		
U1	1	10 / 100 Fast Ethernet 3.3 V transceiver	ST802RT1 FX mode	ST: ST802RT1 FX mode	
U2	1	Fiber optic transceiver	Avago Technologies: AFBR-5803Z	Farnell: 9450025	
U3	1	Linear regulator	LD1117S33	ST: LD1117S33	
X1	1	Epson® Crystal: FA-238	25 MHz	Farnell: 1712818	
Jumper	19	JUMP-SW OPEN BLACK	JUMP-SW OPEN BLACK	GME: 832-140; Farnell: 4218152	

Figure 10. ST802RT1 FX mode Ethernet PHY demonstration board - schematic - part 1

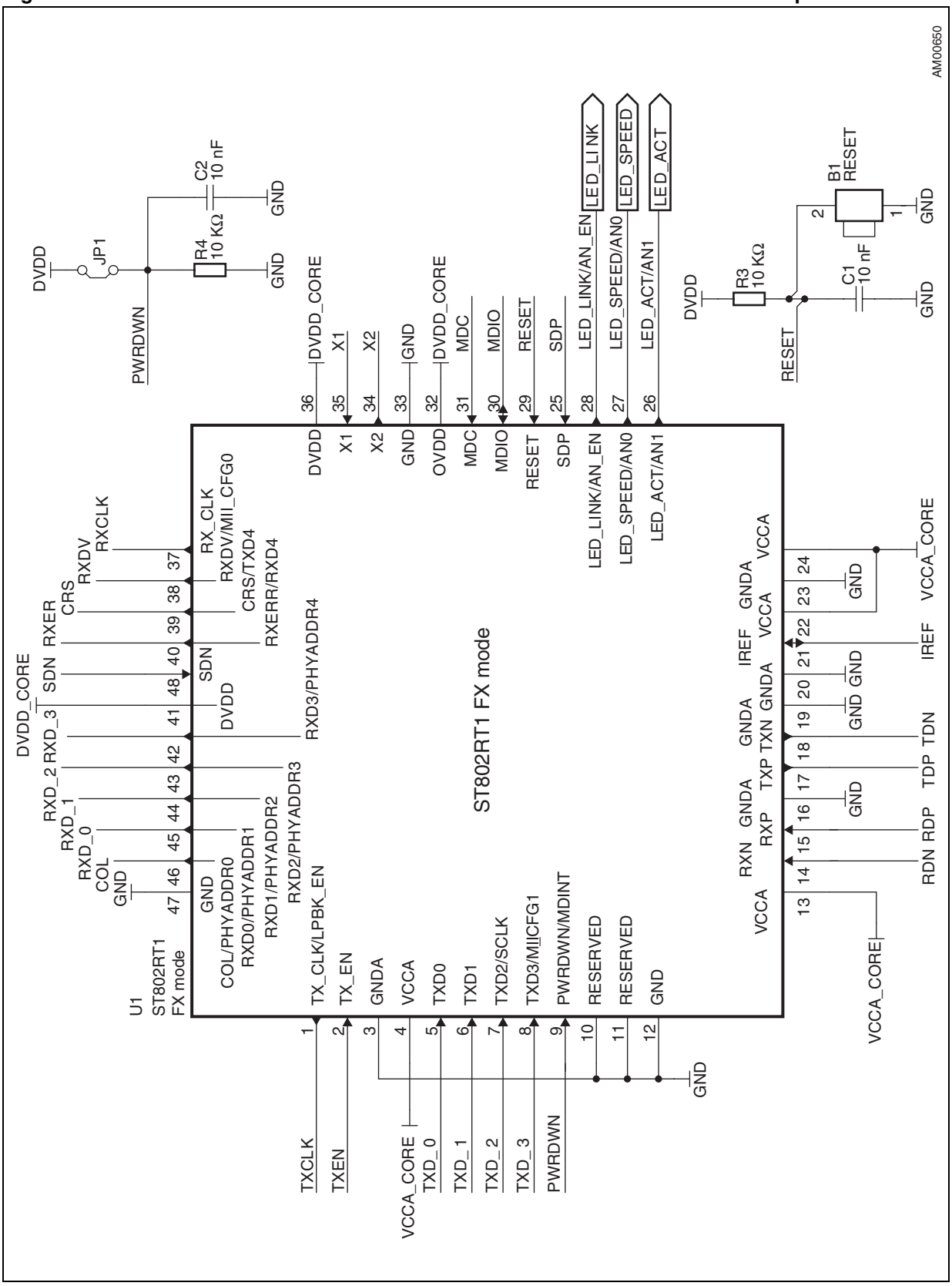


Figure 11. ST802RT1 FX mode Ethernet PHY demonstration board - schematic - part 2

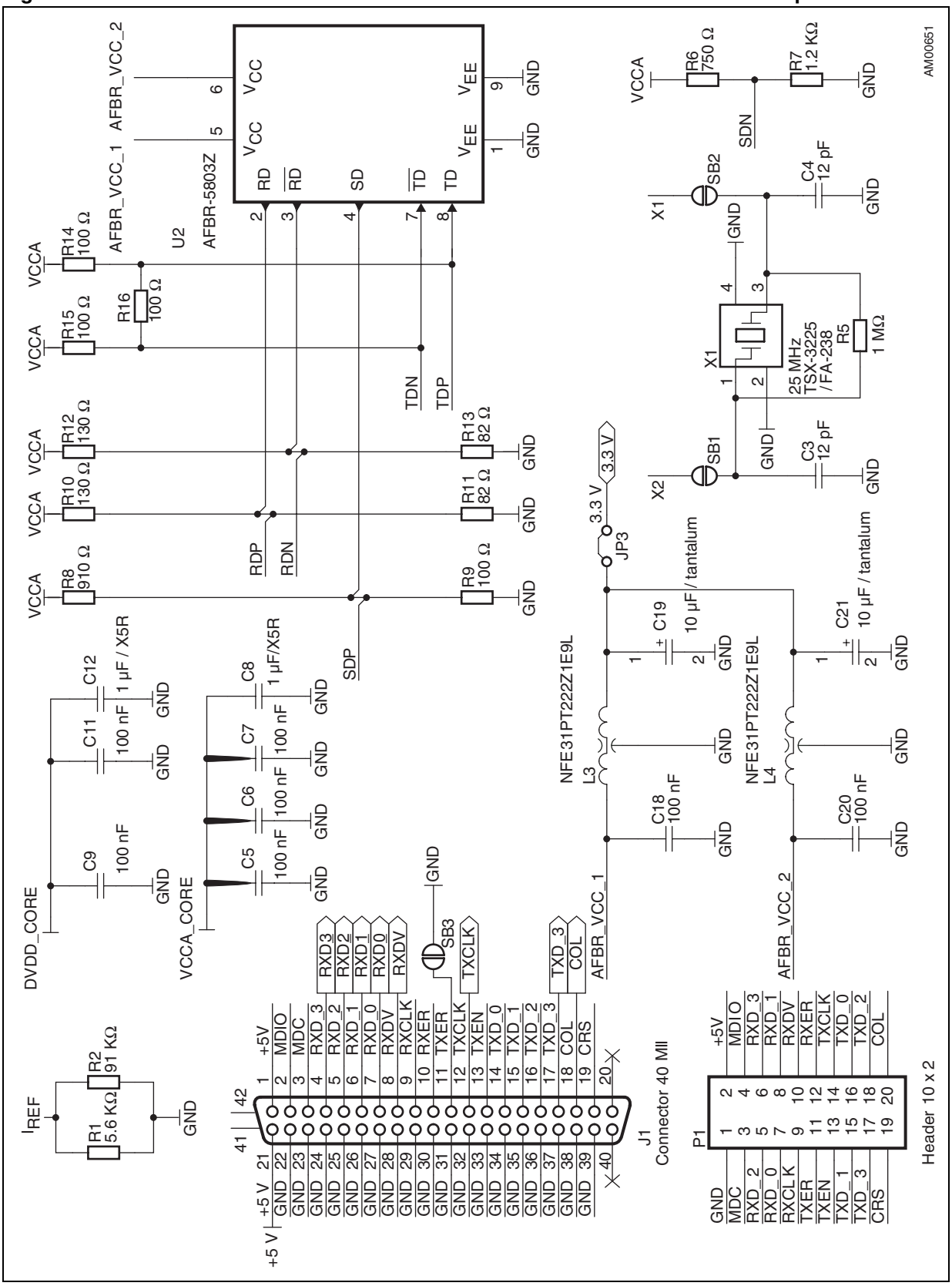
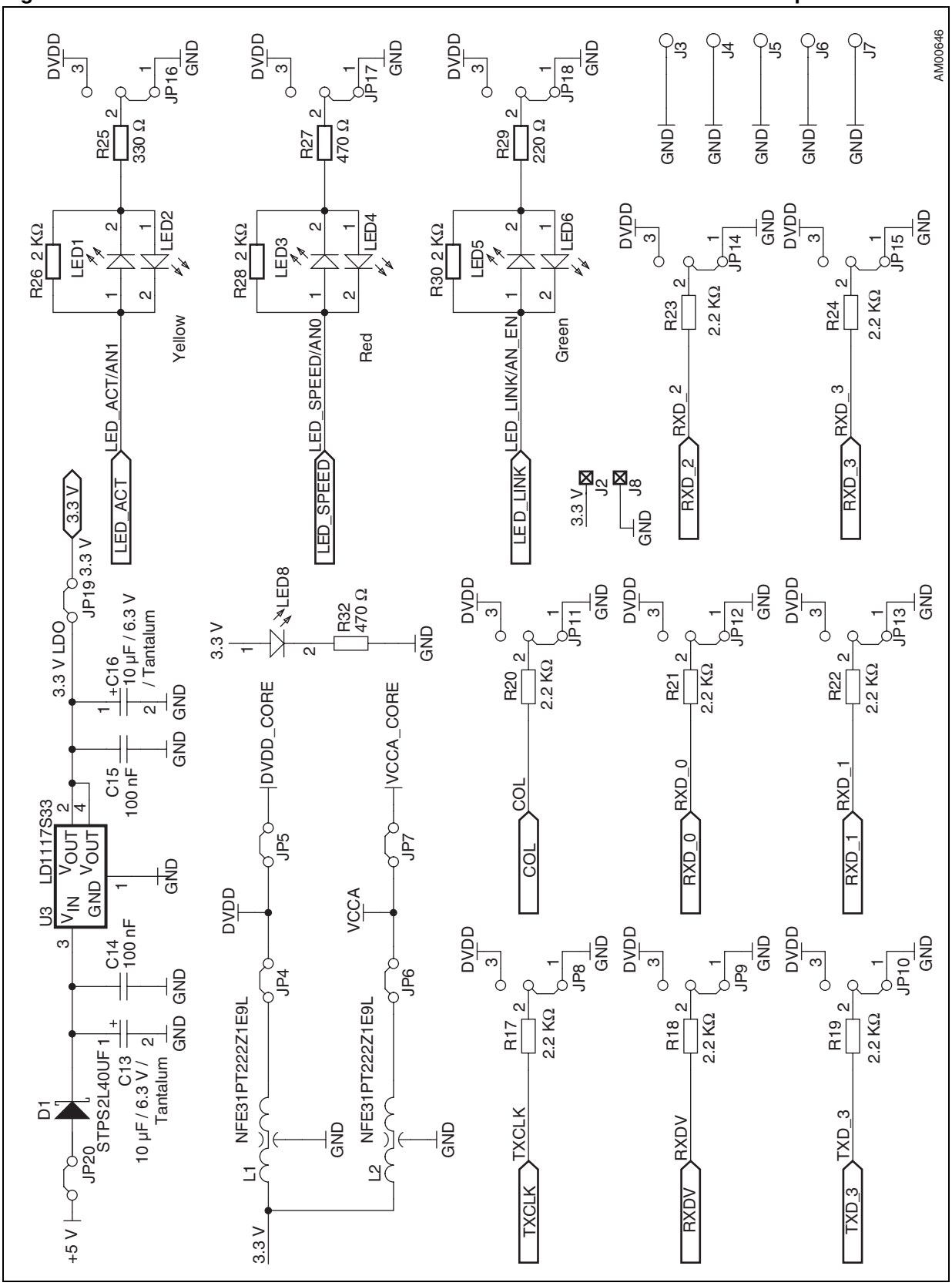


Figure 12. ST802RT1 FX mode Ethernet PHY demonstration board - schematic - part 3



Revision history

Table 14. Document revision history

Date	Revision	Changes
30-Nov-2009	1	Initial release.

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